Claims

1. A method of improving adhesion between an insulating layer and a capping layer in a process for making electronic components comprising:

providing an integrated circuit structure which is in the process of being fabricated into a finished electronic component having an insulating layer;

contacting an exposed surface of said insulating layer with a gas for adsorption of said gas onto said exposed surface of said insulating layer to form a treated surface area of said insulating layer while maintaining an original thickness of said insulating layer;

depositing a capping layer directly over said treated surface area of said insulating layer; and

continuing the process for making the integrated circuit device,

wherein said treated surface area of said insulating layer improves adhesion between said insulating layers and said capping layer to prevent delamination therebetween during said step of continuing the process for making the integrated circuit device.

2. The method of claim 1 wherein said insulating layer has a thickness ranging from about 2,000 Å to about 10,000 Å.

3. The method of claim 1 wherein said insulating layer comprises a low k dielectric.

4. The method of claim 3 wherein said low k dielectric comprises a material selected from the group consisting of organo silicate glass, polyimide, organic siloxane polymer, polyarylene ether, methyle hydrogen, nano-porous silica, hydrogen silesquioxane glass and methyl silesquioxane glass.

5. The method of claim 1 wherein said gas is selected from the group consisting of silane, disilane, dichlorosilane, germane and combinations thereof.

6. The method of claim 1 wherein adsorbed gaseous particles selected from the group consisting of molecules, radicals, derivatives and combinations thereof of said gas are adsorbed onto said exposed surface of said insulating layer to form said treated surface area.

7. The method of claim 6 wherein said adsorbed gaseous particles are adsorbed onto said exposed surface of said insulating layer by heating said integrated circuit having said insulating layer to a temperature ranging from about 100°C to about 500°C and then flowing said gas over said exposed surface of said heated insulating layer.

8. The method of claim 7 wherein said gas is flown over said exposed surface of said heated insulating layer at a pressure ranging from about 0.5 Torr to about 10 Torr for a duration of about 50 sccm to about 500 sccm.

9. A method of forming a semiconductor device comprising:

providing a substrate layer;

depositing an insulating layer over said substrate layer;

heating said substrate layer and said insulating layer;

flowing a treatment gas over a surface of said heated insulating layer;

contacting said surface of said heated insulating layer with said treatment gas for adsorption of said gas onto said surface of said insulating layer to form a treated surface area of said insulating layer while maintaining an original thickness of said insulating layer; and

depositing a capping layer directly over said insulating layer wherein said treated surface area of said insulating layer improves adhesion between said insulating and said capping layers to prevent delamination therebetween during subsequent processing steps.

10. The method of claim 9 further including the step of depositing a dielectric layer over said substrate layer followed by depositing said insulating layer over said dielectric layer.

11. The method of claim 10 wherein said dielectric layer is deposited to a thickness ranging from about 300 Å to about 800 Å.

12. The method of claim 9 wherein said insulating layer comprises a low k dielectric selected from the group consisting of organo silicate glass, polyimide, organic siloxane polymer, polyarylene ether, methyle hydrogen, nano-porous silica, hydrogen silesquioxane glass and methyl silesquioxane glass.

13. The method of claim 12 wherein said insulating layer is deposited to a thickness ranging from about 2,000 Å to about 10,000 Å.

14. The method of claim 9 wherein said substrate layer and said insulating layer are heated and maintained at a temperature ranging from about 100°C to about 500°C.

15. The method of claim 9 wherein said adsorption of said gas onto said surface of said insulating layer comprises adsorbed gas particles selected from the group consisting of gaseous molecules, radicals, derivatives thereof and combinations thereof.

16. The method of claim 9 wherein said treatment gas is selected from the group consisting of silane, disilane, dichlorosilane, germane and combinations thereof.

17. The method of claim 16 wherein said treatment gas is flown over said surface of said heated insulating layer at a pressure ranging from about 0.5 Torr to about 10 Torr.

18. The method of claim 17 wherein said treatment gas is flown over said surface of said heated insulating layer for a duration of about 50 sccm to about 500 sccm.

19. The method of claim 9 further including the step of oxidizing said treated surface area of said insulating layer prior to depositing said capping layer.

20. The method of claim 9 further including the step of carbonizing said treated surface area of said insulating layer prior to depositing said capping layer.

21. The method of claim 9 wherein said capping layer is selected from the group consisting of silicon oxide, silicon carbide and silicon nitride.

22. The method of claim 9 wherein said subsequent processing steps, further including the steps of:

forming a first set of openings in a first mask deposited over said capping layer;

transferring said first set of openings into said insulator layer to form via openings in said insulator layer;

depositing photo resist in an amount sufficient to at least fill said via openings in said insulator layer; and

etching back said photo resist so as to leave remaining portions of said photo resist only within said via openings to form photo resist plugs in said insulator layer.

23. The method of claim 22 further including the subsequent steps of:

forming a second set of openings in a second deposited mask directly over said via openings;

transferring said second set of openings into said insulator layer to form trench openings over said via openings in said insulator layer;

removing said photo resist plugs to expose a metal region of said substrate layer;

depositing a metallization layer in an amount sufficient to at least fill said via openings and said trench openings; and

planarizing a surface of the semiconductor device wherein said treated surface area of said insulating layer prevents delamination between said insulating layer and said capping layer.

24. An intermediate semiconductor structure comprising:

a substrate layer;

an insulator layer disposed over said substrate layer;

a treated surface area of said insulator layer having adsorbed gaseous particles thereon; and

a capping layer disposed over said treated surface area of said insulator layer, wherein said treated surface area prevents delamination between said insulator layer and said capping layer.

25. The intermediate semiconductor structure of claim 24 further including a dielectric layer disposed between said substrate layer and said insulator layer.

26. The intermediate semiconductor structure of claim 24 wherein said insulating layer has a thickness ranging from about 2,000 Å to about 10,000 Å.

27. The intermediate semiconductor structure of claim 26 wherein said insulating layer comprises a low k dielectric material selected from the group consisting of organo silicate glass, polyimide, organic siloxane polymer, polyarylene ether, methyle hydrogen, nano-porous silica, hydrogen silesquioxane glass and methyl silesquioxane glass.

28. The intermediate semiconductor structure of claim 27 wherein said adsorbed gaseous particles are selected from the group consisting of particles of a silane gas, a disilane gas, a dichlorosilane gas, a germane gas and combinations thereof.

29. The intermediate semiconductor structure of claim 27 wherein said capping layer is selected from the group consisting of silicon oxide, silicon carbide and silicon nitride.